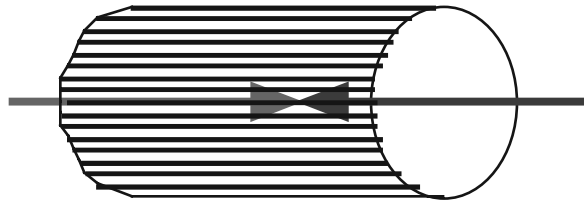


A Fast, First Level Hardware Trigger for the D0 Central Fiber Tracker

by

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- **D0 Detector at Fermilab is being upgraded for TeV II Running**
- **New Tracker for higher luminosity**
- **Scintillating Fiber Tracker part of the upgrade, CFT**
- **Fast, First level trigger from CFT as seed for other triggers.**

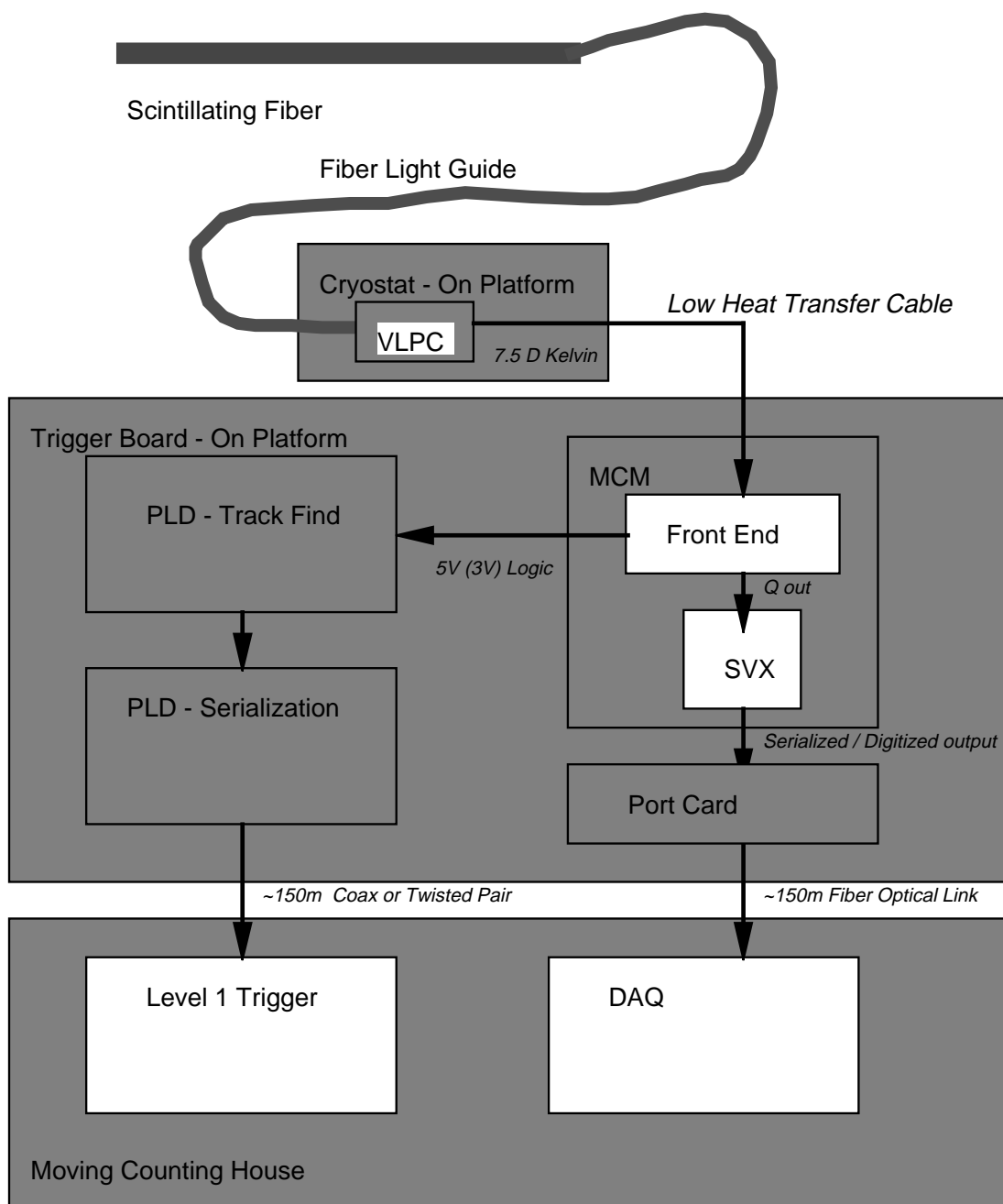
Trigger Requirements::

- **Crossing Every 132 nsec**
 - ⇒ $\langle n \rangle = 1.8$ events per crossing
 - ⇒ about 25 tracks per event
- **Look at Each Crossing**
 - ⇒ Pipeline events
- **Produce Result in < 500 nsec**
 - ⇒ Small Latency
- **Many Channels**
 - ⇒ 38,400 fibers in trigger
- **Be Able to Adjust Algorithm**
 - ⇒ Changes in Physics Interest
 - ⇒ Systematic Variations in as-built detector
- **Keep Cost Low**

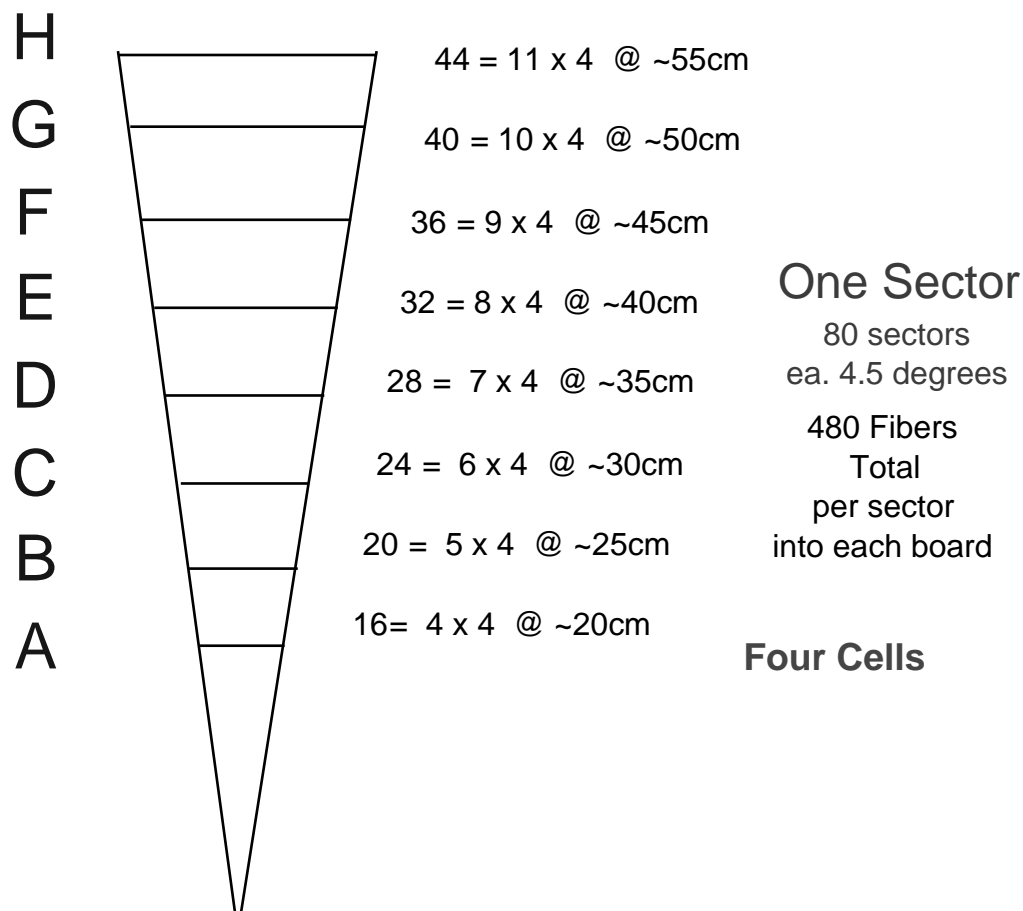
◇ **USE FPGA**

- ⇒ Massively Parallel
- ⇒ Fast Logic
- ⇒ Re-programmable (in place)
- ⇒ Commercial product - Market pressure on cost/features enhancement

Central Fiber Tracker { CFT } Data Flow



Fiber Arrangements for Trigger



- Each PCB has fiber channels from a pie shaped sector
- All the channels needed to form a trigger are in the 'Home Sector' or either of two 'Neighbor Sectors'.

- **Require all 8 of 8 layers have a hit**

⇒ Needed to reject fakes

- **Narrow Roads**

⇒ Needed to reject fakes

⇒ Pushes up Number of Equations

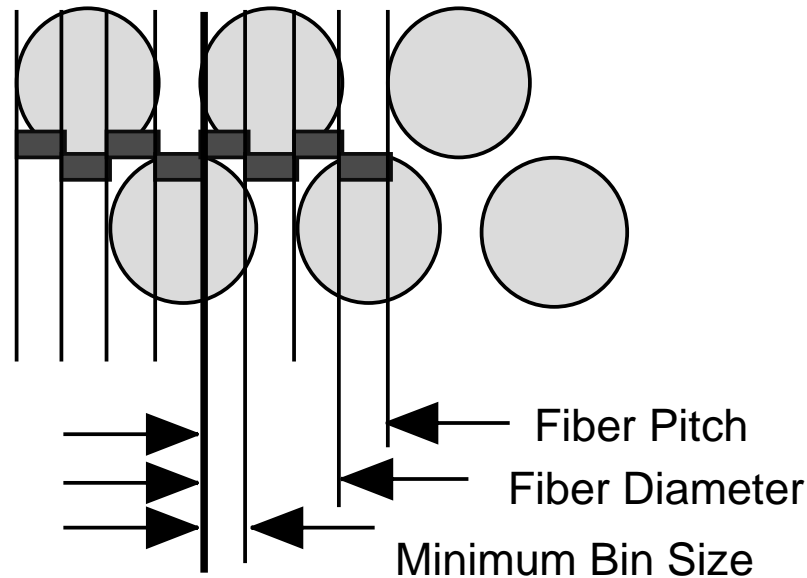
- **Lowest Pt Possible**

⇒ Pushes up number of equations

◇ **Based on MC simulations => 1 fiber wide bins**

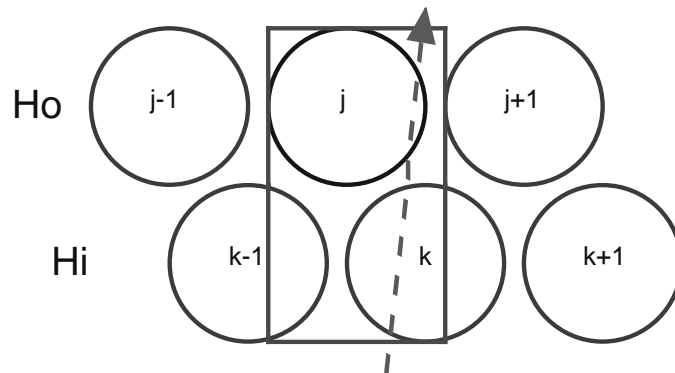
<u>Threshold</u>	<u>Number of Equations</u>
6 GeV	1100 per cell / 4400 per sector
3 GeV	2200 per cell / 8800 per sector
1.5 GeV	3300 per cell / 13,200 per sector

Forming Doublets



Two single layers are offset by about $\frac{1}{2}$ fiber so there are no cracks

This offset character can be used to define different Doublet bin sizes



We make the Doublet bin size equal 1 fiber pitch

The equation for doublet bin j is:

$$HI[j] = (\text{NOT}(Ho[j+1]) \text{ AND } Hi[k]) \text{ OR } Ho[j];$$

Note that when a track passes through $Hi[k]$ and $Ho[j+1]$, $HI[j]$ will be FALSE and only $HI[j+1]$ will be TRUE.

Forming Tracks

First use equations to find 8 of 8 hits along each road:

$$T_{1013172227323945} = AL[10] \text{ AND } BL[13] \text{ AND } CL[17] \text{ AND } \\ DL[22] \text{ AND } EL[27] \text{ AND } FL[32] \text{ AND } GL[39] \text{ AND } HL[45];$$

The index numbers 10, 13, ... depend upon the details of the design

The several terms that share
 inner - a phi bins and
 outer - h phi bins

are OR'ed together

$$\text{Trig_a10h45} = T_{\underline{10}131722273239\underline{45}} \text{ OR } T_{10\dots45} \text{ OR } \dots$$

These terms are then OR'ed together into Pt bins

$$\text{Trig_p7h45} = \text{Trig_a10h45} \text{ OR } \text{Trig_a11h45} \text{ OR } \dots$$

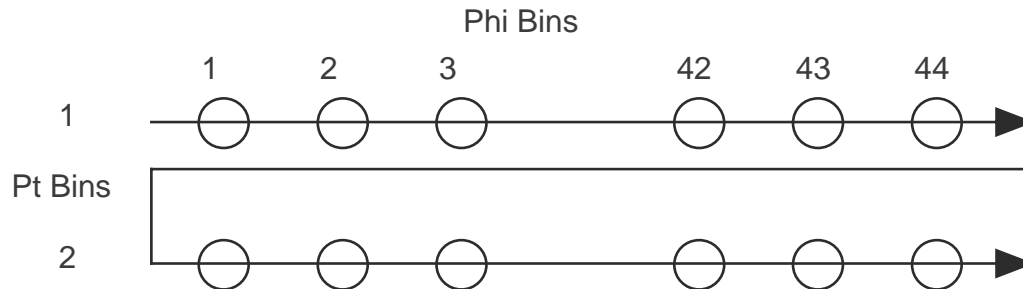
h45 => Phi bin 11 per cell / 44 per sector

p7 => Pt bin 8 Pt bins

88 Outputs

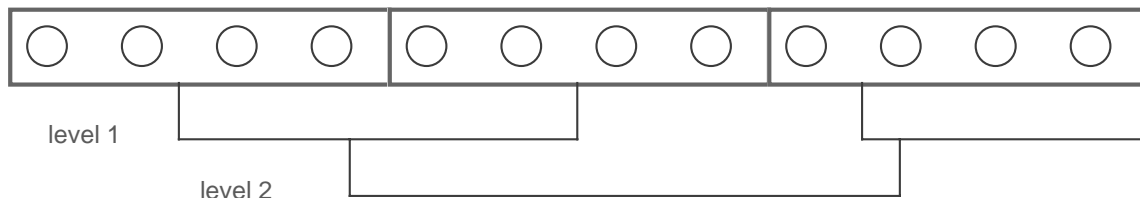
Serialization of Output

- ◆ Required output is list of first 6 hits in Pt order
- ◆ Each hit has a 6 bit phi address and 3 bit Pt bin identifier



- Sort results into a list of hits ordered by Pt (within phi bins)
- Sort two Pt bins in each FPGA - 4 FPGAs used for 8 Pt bins
- Sort through 88 inputs

Serial Sort would require too much time - too many cycles



- Start Sort by putting groups of 4 into Truth Tables to create 22 lists
- Concatenate lists by pairs - 5 levels required to reach one list

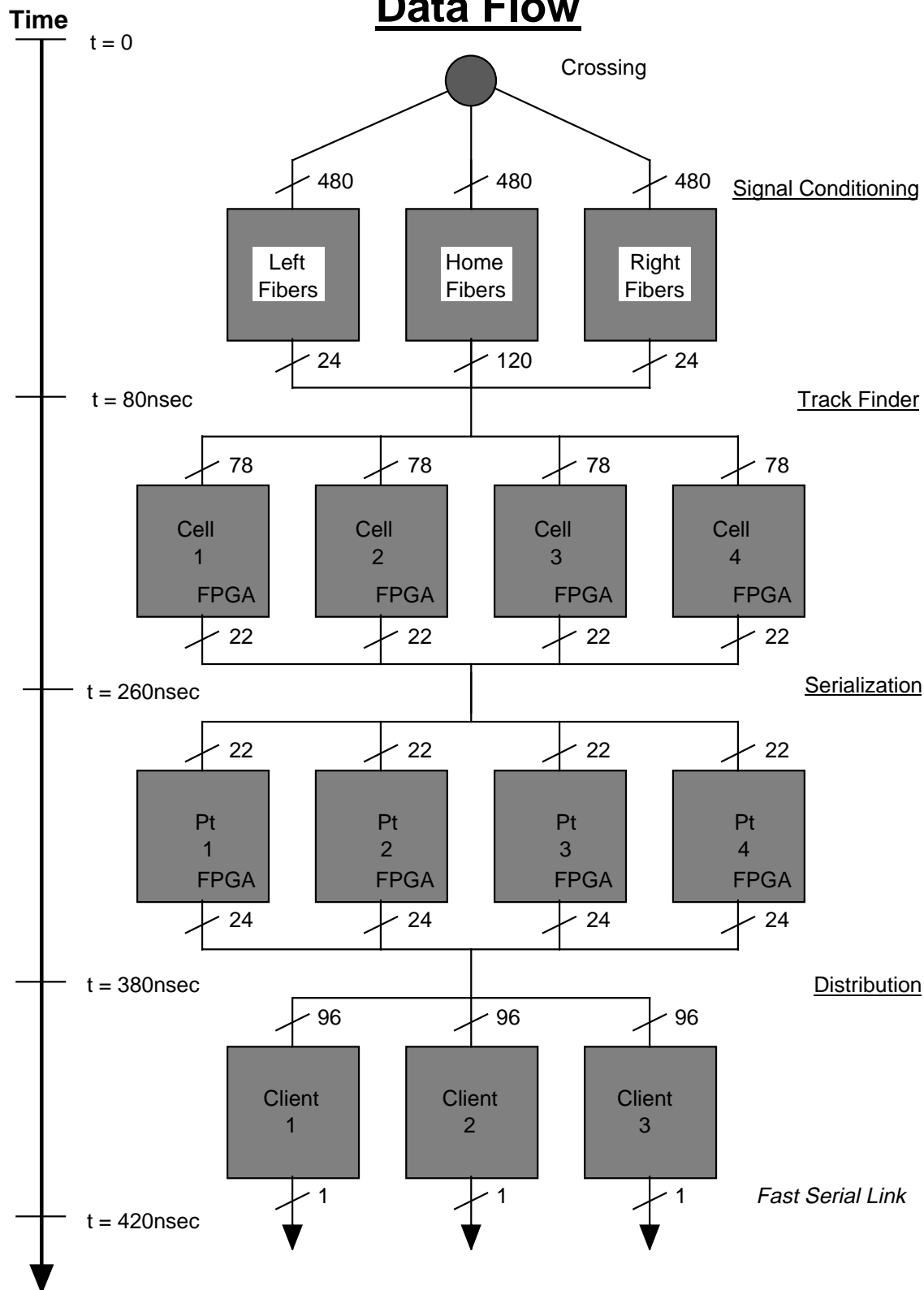
Distribution of Information

- ◆ Concatenate input lists
- ◆ Extend hit addresses to 16 bits each
- ◆ Add header word

Header
address hit 1
address hit 2
address hit 3
address hit 4
address hit 5
address hit 6

- Continuously broadcast over copper, fast serial link
- 16 bits every 18.8 nsec
- 7 words (/ one crossing of data) every 132 nsec (/ every crossing)

Schematic of Data Flow



Entire Process takes 420 nsec

80 nsec	Signal Conditioning
180 nsec	Track Finding
120 nsec	Serialization
40 nsec	(Start of) Distribution

Entire Process requires about 10 large FPGAs

4	Track Finding
4	Serialization
1-2	Distribution / Control

Use about 70,000 gates in each FPGA**Total Project requires 800 FPGAs**